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Result # 1 Relevance:

Emulation of Switch to Supervisor

1998-07-01 IPCOM000123239D English

A method to allow privileged operating system code to execute with non-privileged acc where no hardware facilities exist to support such operation.

Result # 2 Relevance:

MATE: Micro Assist Thread Engine

2004-04-07 IPCOM000027405D English

We disclose POWERmate, an asynchronous PowerPC assistive processing facility based infrastructure. Using the the assistive thread facility, asynchronous threads can be exec multiple thread contexts on a single (or multiple) processor cores. The ...

Result # 3 Relevance:

Use of a Hardware Monitor to Create Send/Receive within CSRs

1993-09-01 IPCOM000105704D English

Given a sequential program the task of creating a set of CSRs that execute the progran requires that memory accesses among shared data be coordinated using SEND/WAIT&I use of a hardware monitor to assist in this task provides the means of ...

Result # 4 Relevance:

Precise Interrupt Handling for Out-of-Order Instruction Execution

1999-09-01 IPCOM000123996D English

A new interrupt processing method for out-of-order executed instructions on superscal systems is introduced. It provides precise interrupt reporting as required for a lot of co architectures.

Result # 5 Relevance:

Efficient Task Switching With An Off-Load Processor

1979-11-01 IPCOM000068186D English

One method of increasing the performance of a computing system involves increasing t processors performing the work. The usual approach has been to provide multiple proc in some sense symmetric, both executing both system and application code. ...

Result # 6 Relevance:

Method for dynamic lockout avoidance in a SMT processor

2005-01-04 IPCOM000033913D English

In a simultaneous multi-threaded (SMT) processor, a thread may become "locked out" from making forward progress by the other thread(s). Disclosed is a method to dynami thread "lockout" by guaranteeing that each thread make ...

Result # 7 Relevance:

Processor Single Step Trace Facility Enhancements

1996-12-01 IPCOM000118286D English

Providing instruction and address traces is a very important part of system tuning and i design. There are many different methodologies for providing this support, each of whi benefits and problems. Disclosed is a reasonably cost-effective approach ...

Result # 8 Relevance:

Use of the SYNC Instruction to Synchronize Completion of Translation Buffer Invalidate in a Multi-Processor System

1994-05-01 IPCOM000112440D English

Disclosed is a hardware solution for synchronization of Translation Look-aside Buffer (T down in a Symmetric Multi-Processor System (SMP). By using the SYNC instruction in c with the TLB Invalidate (TLBI) instruction, a method is described to ensure ...

Result # 9 Relevance:

Wiring SPR out to hardware in-memory trace for a programmable sof capability

2005-05-04 IPCOM000124721D English

Most modern processors contain specialized hardware to record hardware performance occur during instructions processing. These traces can be collected form processor core buses. Typically hardware traces provide data used to simulate system ...

Result # 10 Relevance:

Processor supporting asymmetric multithreading capability

2002-08-11 IPCOM000016150D English

Described is a microprocessor with multithreading capabilities. Typical multithreading d to replicate the entire processor state for all supported hardware threads, including, bu to, integer, floating point, condition registers segment ...

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Search query: A virtual multithreading hardware mechanism provides multi-threading on a s processor. Thread switches are triggered by user-defined triggers. Synchrono defined in the form of special trigger instructions. Asynchronous triggers may special marking instructions that identify an asynchronous trigger condition. T trigger condition may be based on a plurality of atomic processor events. Min information, such as only an instruction pointer address, is maintained by the thread switch. In contrast to traditional simultaneous multithreading schemes multithreading hardware provides thread switches that are transparent to an and that may be performed without operating system intervention.

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